**Cell Description:**This is a standard NAND cell with the following Boolean equation.

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Behavioral Verilog:**The behavioral Verilog for the NAND is independent of its drive strength. Replace the N in the module name with the respective drive strength (i.e. 1, 2).

//Verilog HDL for "Lib6710\_06", "NAND2X1" "behavioral"

module NAND2X1 ( Y, A, B );

output Y;

input A;

input B;

nand \_i0(Y, A, B);

specify

(A => Y) = (1.0, 1.0);

(B => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| NAND2X1 | 27.0 | 7.2 |
| NAND2X2 | 27.0 | 7.2 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Logic Symbol:**

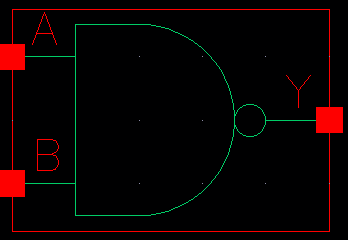
****

Figure 1: Symbol View for the NAND cell.

**CMOS Schematic:**The following figure displays the CMOS schematic for the NAND cell with a 1 times drive strength (NAND2X1), all drive strengths have the same schematic with transistor widths that scale by the drive  
 strength factor (i.e. the width of the PMOS in the NAND2X2 is 6.0μM and the NMOS width is 6.0μM) .

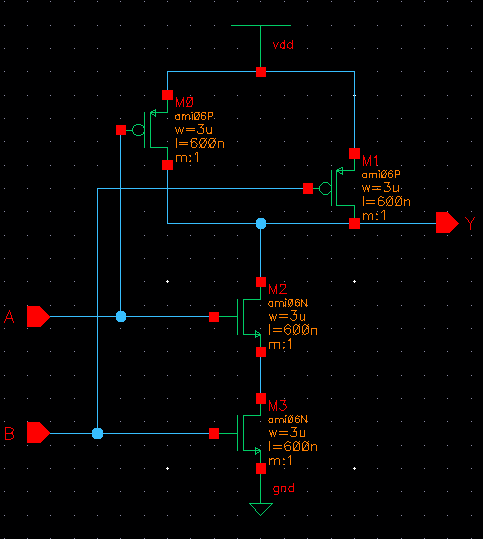


Figure 2: CMOS Schematic for the NAND2X1 cell.

**CMOS Layout:**

The following figures display the CMOS layouts for the NAND cells.



Figure 3: CMOS layout for the NAND2X1 cell.



Figure 4: CMOS layout for the NAND2X2 cell.